

# **AlSb/InAs HEMTs and their Integration with RITDs**

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3rd Workshop on the Fabrication,  
Characterization, and Applications of  
6.1Å III-V Semiconductors

July 31, 2001

This work was supported by the  
Office of Naval Research

# Low-Voltage, High-Speed AlSb/InAs HEMTs

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- **Objective:**

- Develop advanced InAs HEMT technology which will lead to lower noise figure, higher gain, and lower power consumption in microwave/mm-wave receivers and high-speed logic circuits.

- **Technical Approach:**

- Resolve fundamental material and design issues which are unique to the AlSb/InAs material system.
- Develop design and fabrication methods to fully realize the performance potential of the system.

# Personnel

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- **MBE growth** Brian Bennett, Ben Shanabrook, Allan Bracker, Ming J. Yang
- **MBE characterization** Brian Bennett, Ming J. Yang, Rich Magno, Allan Bracker
- **E-beam lithography** Doe Park, Bob Bass
- **HEMT fabrication** Brad Boos, Doe Park, Wontae Chang
- **HEMT measurements** Brad Boos, Walter Kruppa, Rich Magno, Wontae Chang  
Jeff Mittereder, and N. H. Turner
- **Wafer bonding** Karl Hobart, Fritz Kub
- **RTD/HEMT integration** Brad Boos, Rich Magno, Mario Ancona
- **Simulation** Mario Ancona, Walter Kruppa, Ming J. Yang, Brad Boos,  
Eric Justh



# Outline

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- Background
- InAsSb channel HEMTs
- TiW/Au gate HEMTs
- $1/f$  noise characterization
- RITD/HEMT integration
- GaSb transferred substrates
- Summary

# Potential Applications

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**High-speed, low-power consumption electronics needed for light-weight power supplies, extension of battery lifetimes, and high data rate transmission.**

- **Low-noise receivers**
  - space-based sensing and communications
  - portable communications
  - micro-air-vehicles (MAVs)
- **High-speed logic circuits**
  - communications, data transmission
  - potential for lowest power-delay product
  - integration with Sb-based RTDs for enhanced functionality and low-voltage operation

# AISb/InAs HEMT Motivation

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- **Attractive Material Properties**

- High electron mobility
- High electron velocity
- Large conduction-band offset
- High 2-DEG sheet-charge density

**Potential for High Speed and Low Noise at Low Drain Voltage**

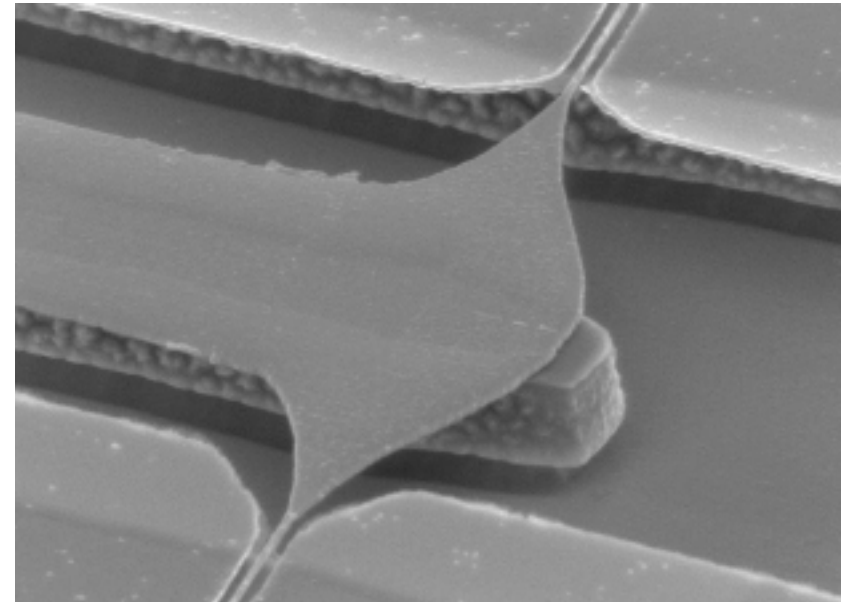
- **Design Issues**

- Impact ionization/High output conductance
- High gate leakage current

# AlSb/InAs HEMT Fabrication

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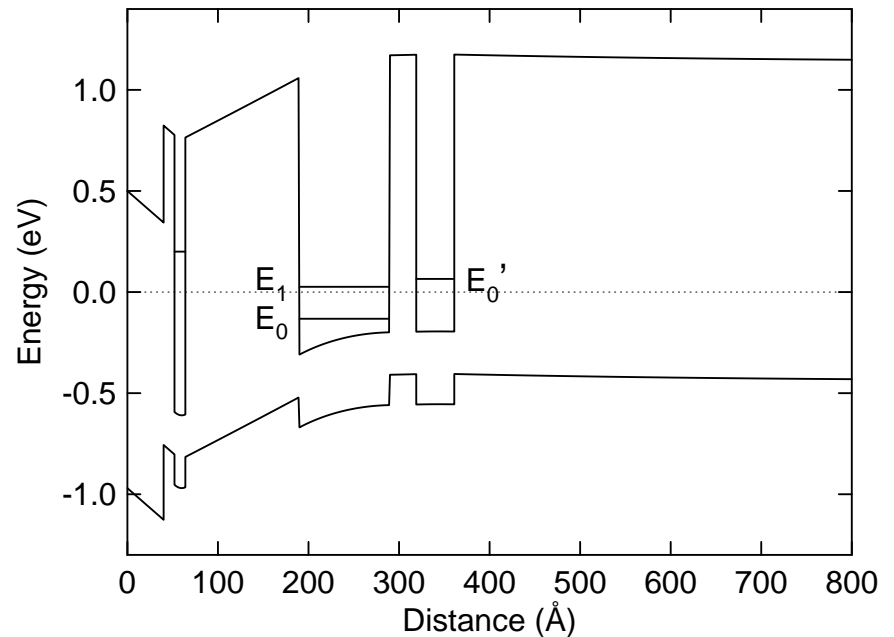
- **Pd/Pt/Au ohmic contacts**
  - Heat-treated at 175°C for 3 hours
  - Pt diffusion barrier
- **InAlAs/AlSb composite barrier**
  - Enables gate recess etch
  - Reduces gate leakage current
  - Reduces kink effect
- **TiW/Au (175Å/1000Å) gate**
  - E-beam lithography
  - Citric acid-based surface treatment
- **Mesa isolation**
  - Hydrofluoric acid-based etch
  - Gate air-bridge at mesa edge



$$L_G = 0.2 \mu\text{m}, L_{DS} = 1.0 \mu\text{m}$$

# Reduced Impact Ionization in HEMTs with an InAs Subchannel

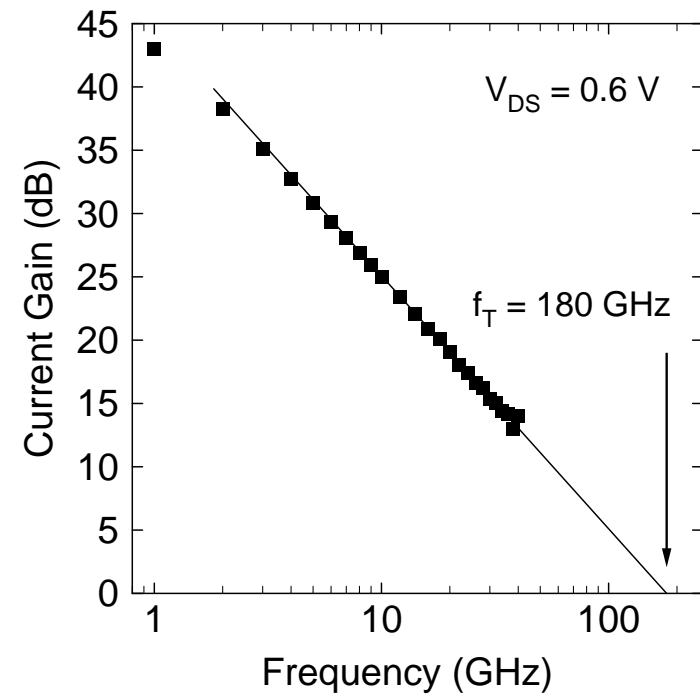
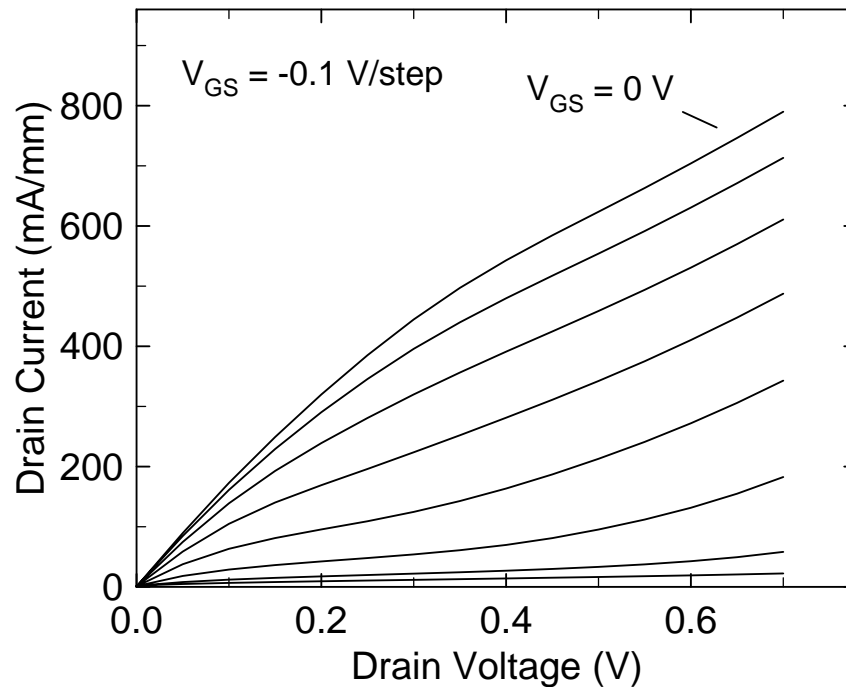
InAs 20 Å
In <sub>0.4</sub> Al <sub>0.6</sub> As 40 Å
AlSb 12 Å
InAs(Si) 12 Å
AlSb 125 Å
InAs 100 Å
AlSb 30 Å
<b>InAs subchannel 42 Å</b>
AlSb 500 Å
p-GaSb(Si) 100 Å
AlSb 2.5 μm
SI GaAs substrate



42 Å InAs subchannel reduces impact ionization by transfer of hot electrons to subchannel which has a larger effective bandgap due to quantization.



# 0.1 $\mu\text{m}$ InAs HEMTs with InAs Subchannel



## Microwave Performance at $V_{DS} = 0.6$ V

$$g_m(\text{rf}) = 850 \text{ mS/mm}$$

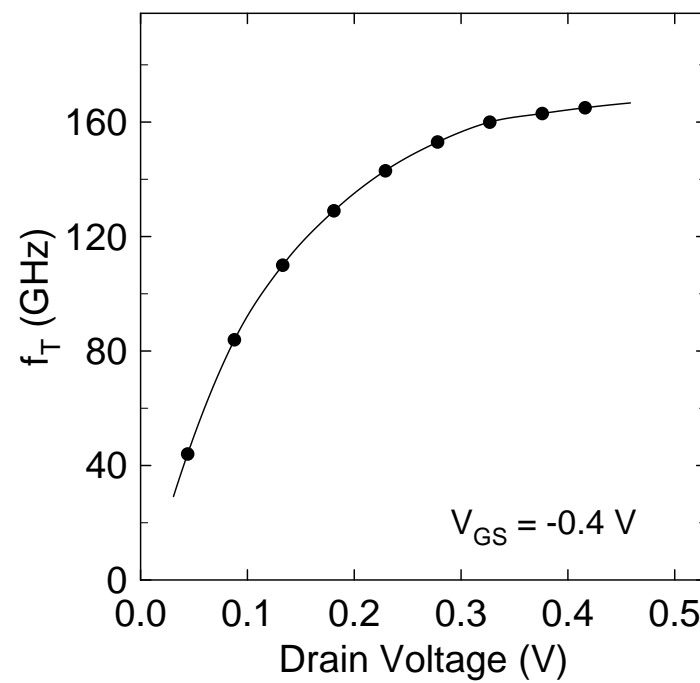
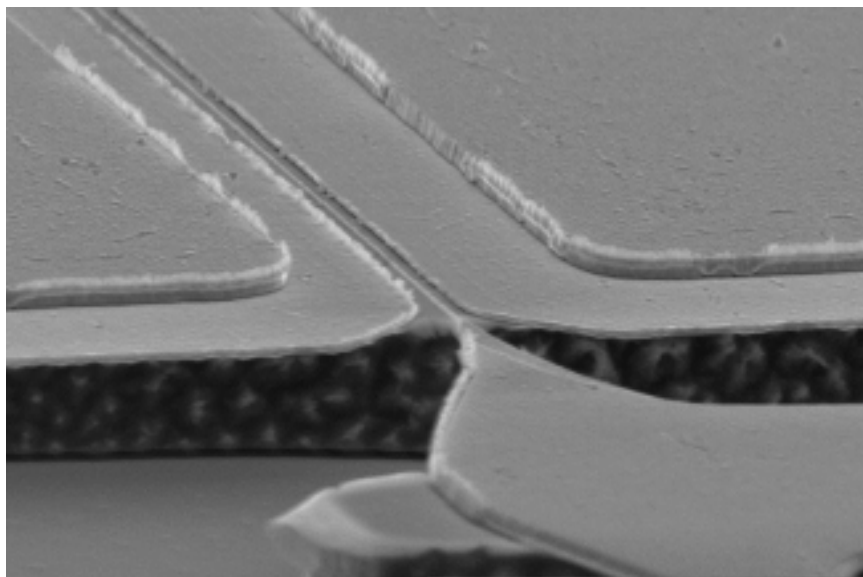
$$f_T = 180 \text{ GHz}, f_{\text{max}} = 80 \text{ GHz}$$

$$f_T = 250 \text{ GHz (after removal of bond pad capacitance)}$$

Ref: *Electron. Lett.*, vol. 34, no. 15, July 1998



# 60 nm InAs HEMT Characteristics



## Microwave Performance at $V_{DS} = 0.35$ V

$$g_m(\text{rf}) = 1 \text{ S/mm}$$

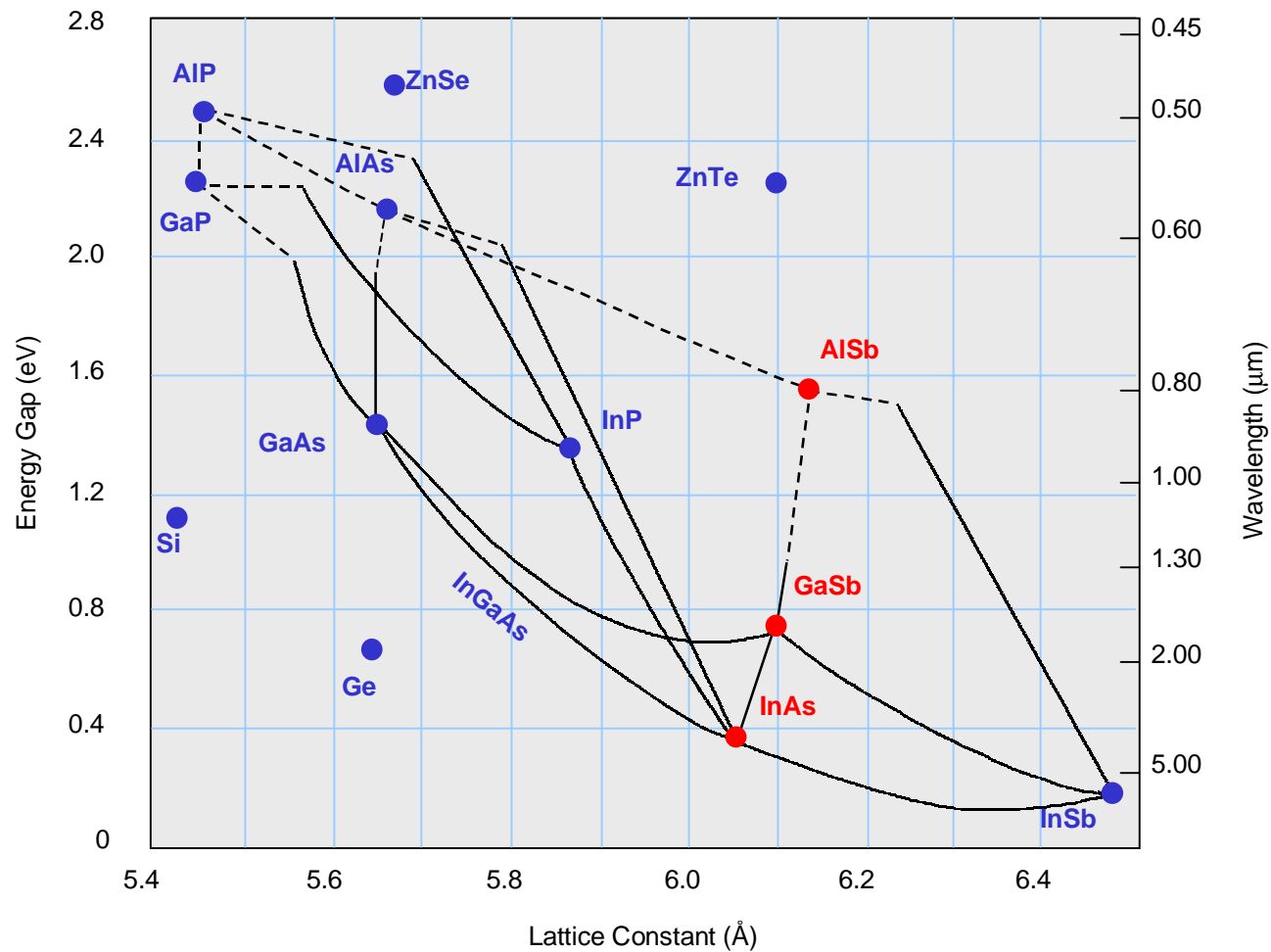
$$f_T = 160 \text{ GHz}$$

$$f_{\text{max}} = 80 \text{ GHz}$$

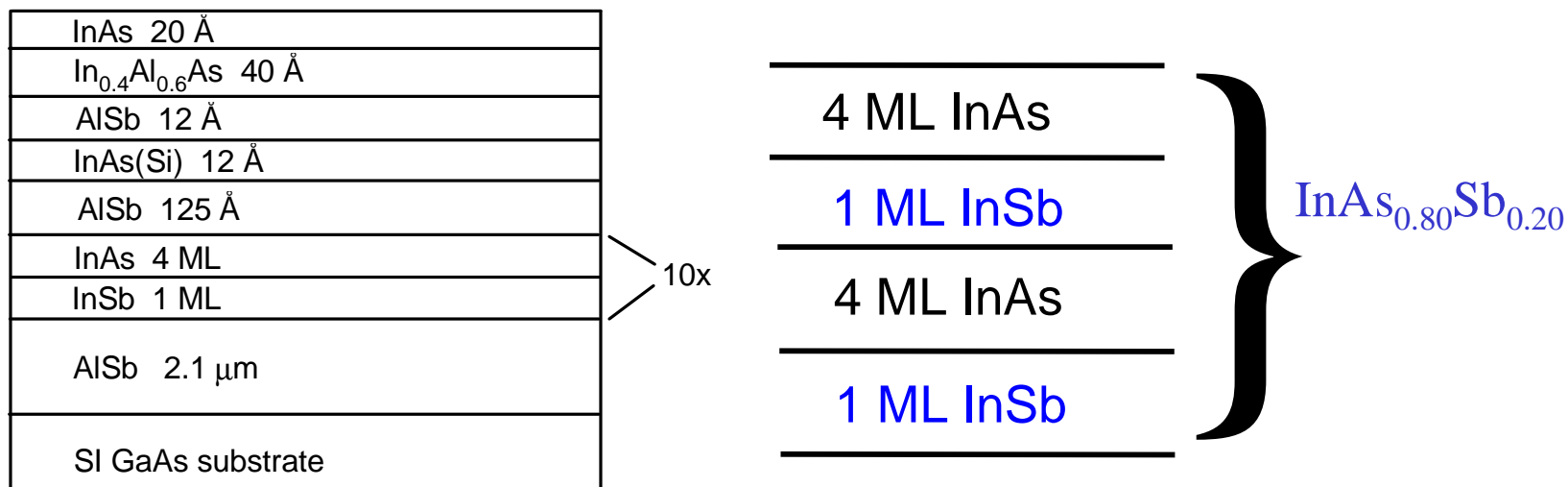
**$f_T = 90$  GHz at 100 mV is highest reported for a FET at this drain bias.**

Ref: *J. Vac. Sci. Technol. B*, 17 (3), May 1999

# AlSb/InAs/GaSb Material System

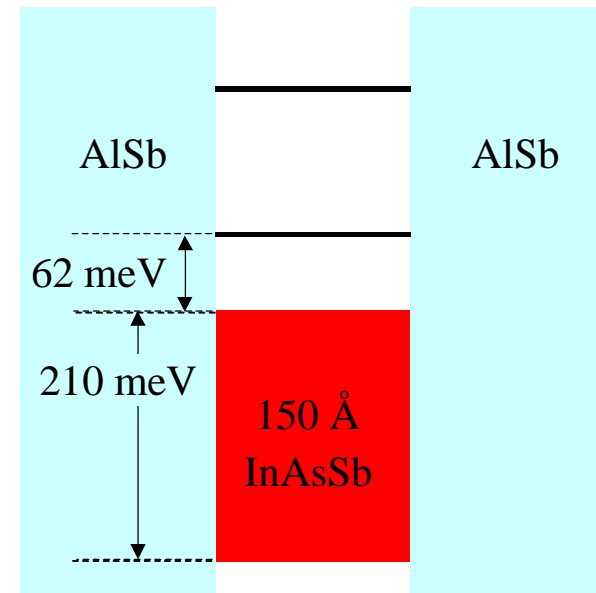
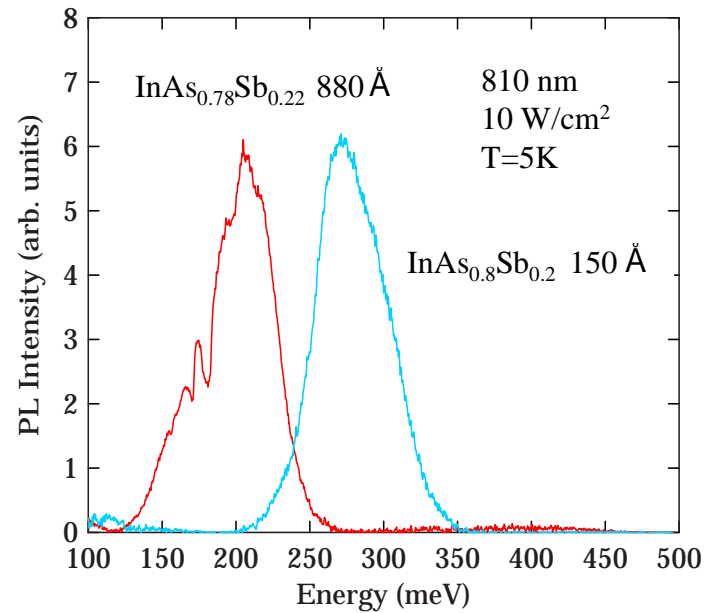


# HEMTs with Digital Alloy $\text{InAs}_{1-x}\text{Sb}_x$ Channel



- $\text{InAs}_{0.8}\text{Sb}_{0.2}$ , which is lattice matched to AlSb, was grown as a digital alloy superlattice with 4 ML InAs / 1 ML InSb.
- AlSb/InAsSb has type-I band lineup.
  - more hole confinement
  - lower output conductance

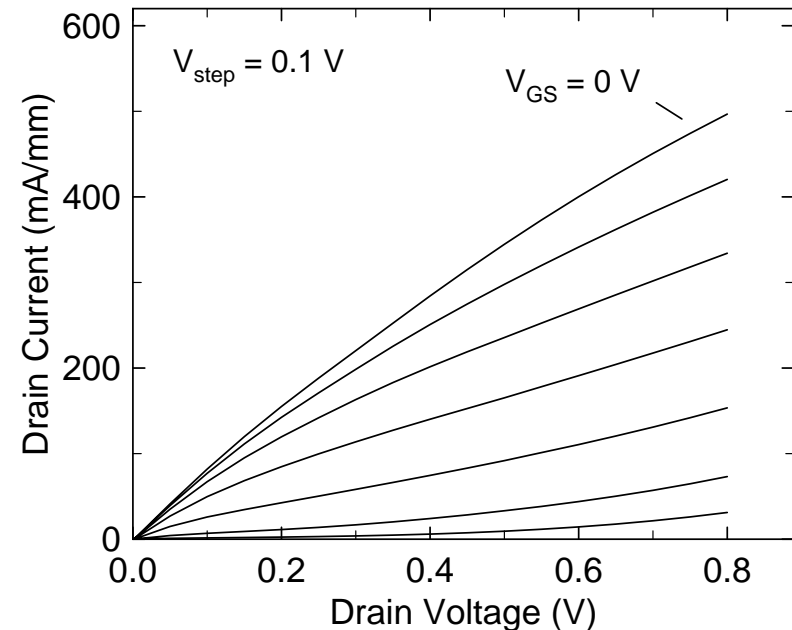
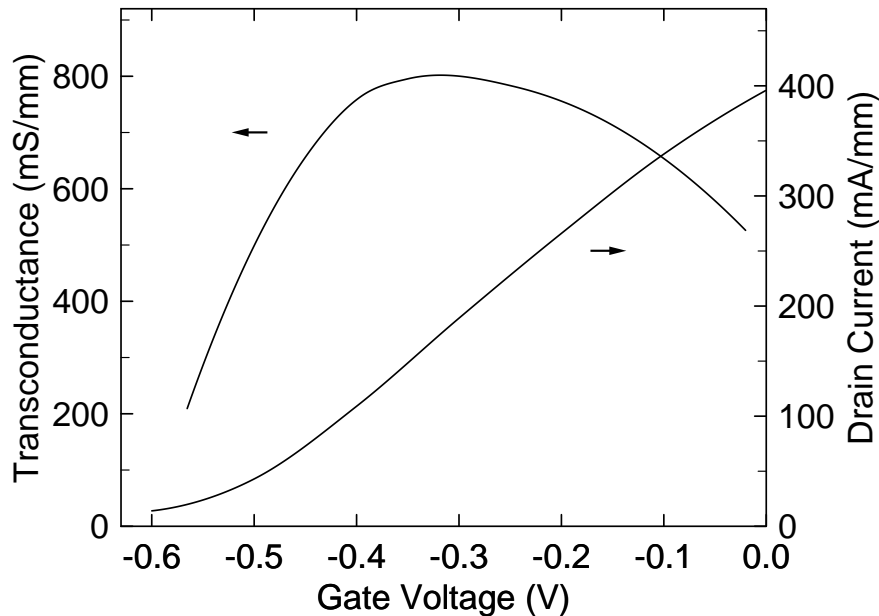
# Type-I Band Offset between AlSb and InAsSb



Photoluminescence measurements show the transition from type-II to type-I band alignment occurs around 15% of Sb.

Ref: *J. Appl. Phys.*, vol. 87, no. 11, June 2000

# 0.1 $\mu\text{m}$ InAsSb HEMT Characteristics

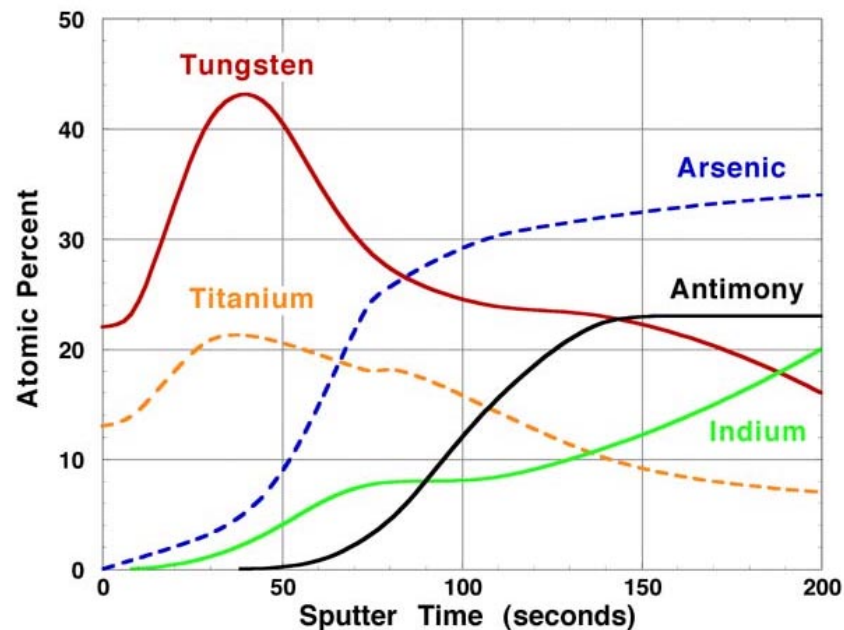


## Microwave Performance at $V_{DS} = 0.6 \text{ V}$

- $f_T = 130 \text{ GHz}$  @  $V_{DS} = 0.6 \text{ V}$
- $f_{T, \text{int.}} = 180 \text{ GHz}$  @  $V_{DS} = 0.6 \text{ V}$
- $g_m = 700 \text{ mS/mm}$ ,  $g_d = 110 \text{ mS/mm}$
- Voltage gain of 6 is highest reported for this material system with this gate length.

# TiW/Au Gate Metalization

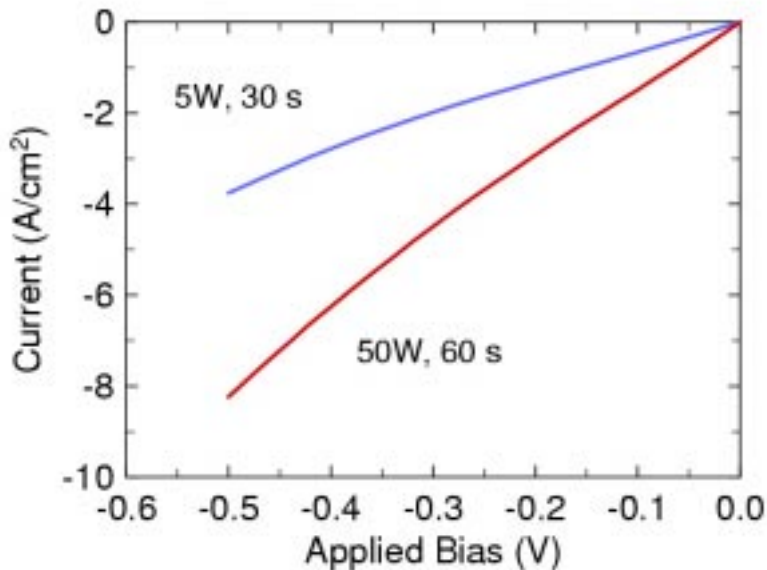
## XPS of TiW Layer



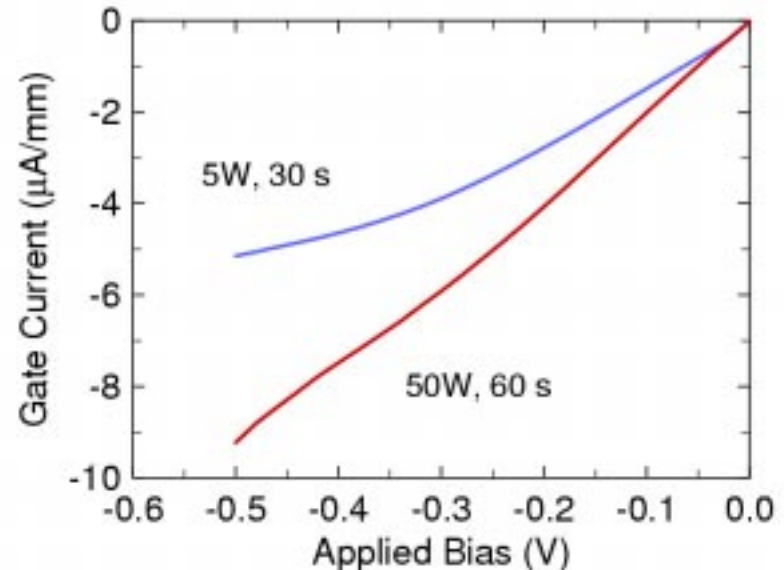
- **TiW/Au gate metalization for increased thermal stability**
  - TiW contacts on GaAs previously shown to be stable to 650°C
  - E-beam evaporated from alloy source (90% W, 10% Ti)
  - XPS indicates deposited layer is 65% W and 35% Ti

# Oxygen Plasma Surface Pretreatment

Bond pad before isolation (3200  $\mu\text{m}^2$ )



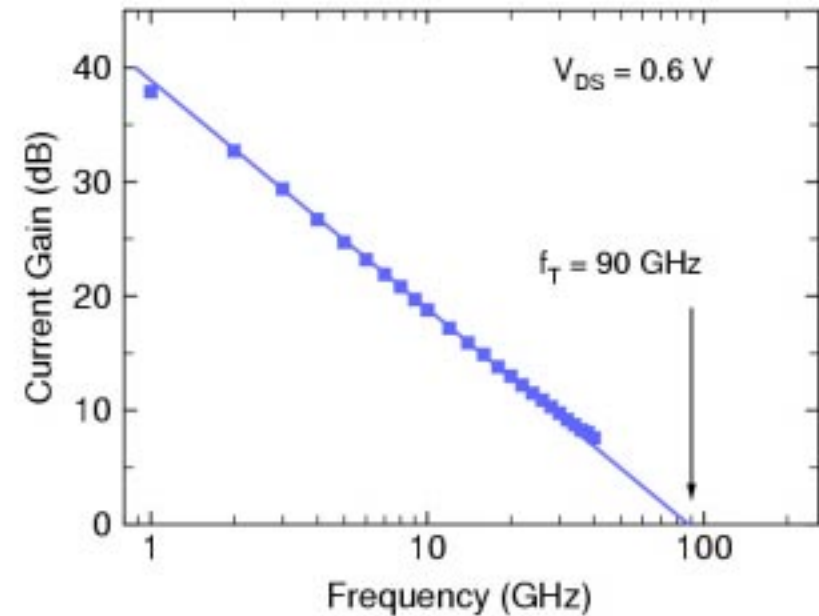
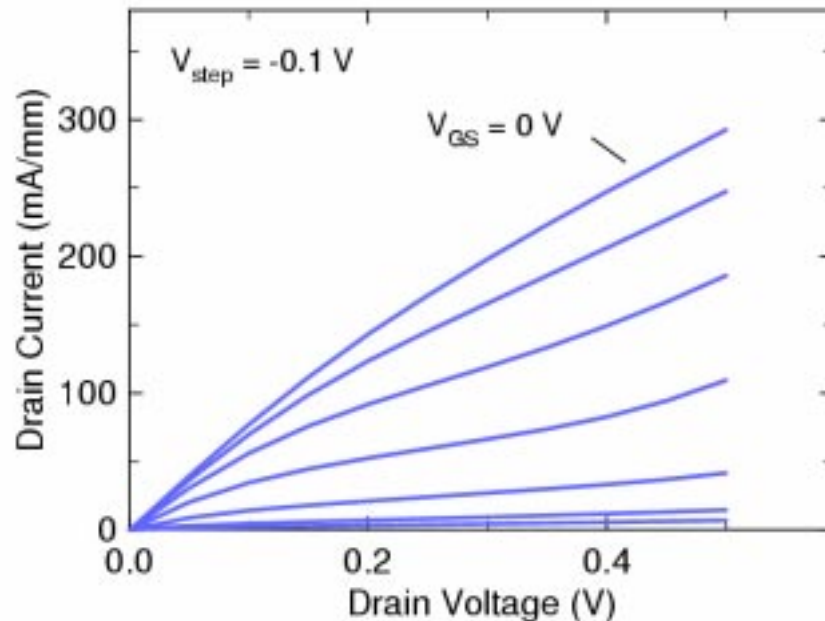
HEMT gate diode after isolation



- **Adjusted oxygen plasma surface pretreatment to reduce damage**
  - Previous treatment: barrel etcher, 50 W for 60 s
  - New treatment: parallel-plate etcher, 5 W for 30 s
  - Diodes with new treatment exhibit 2x lower gate leakage



## 0.2 $\mu\text{m}$ InAs HEMTs with TiW/Au Gate Metal



### HEMT Performance at $V_{\text{DS}} = 0.6 \text{ V}$

$$g_m = 750 \text{ mS/mm}$$

$$f_T = 90 \text{ GHz}, f_{\text{max}} = 80 \text{ GHz}$$

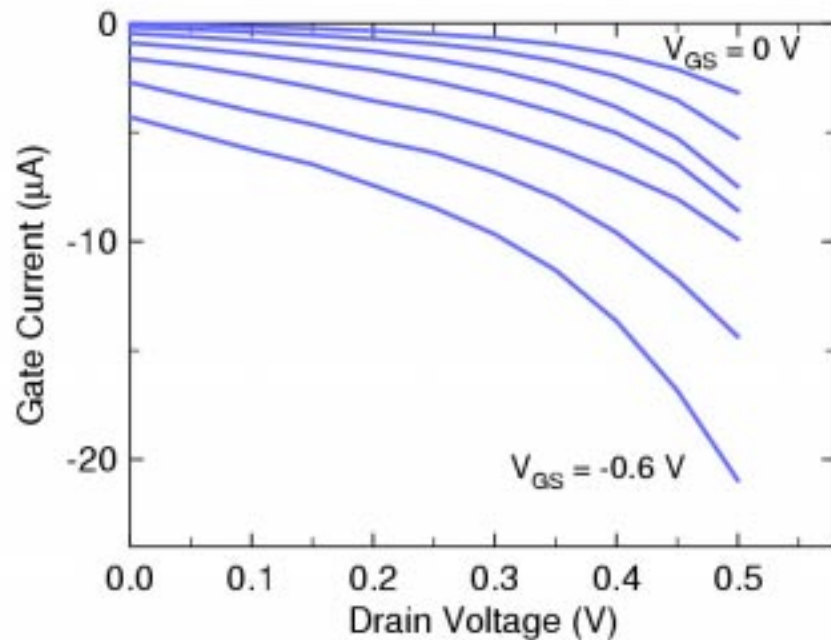
$$f_T = 120 \text{ GHz (after removal of bond pad capacitance)}$$

Ref: *IPRM Proceedings*, May 2001

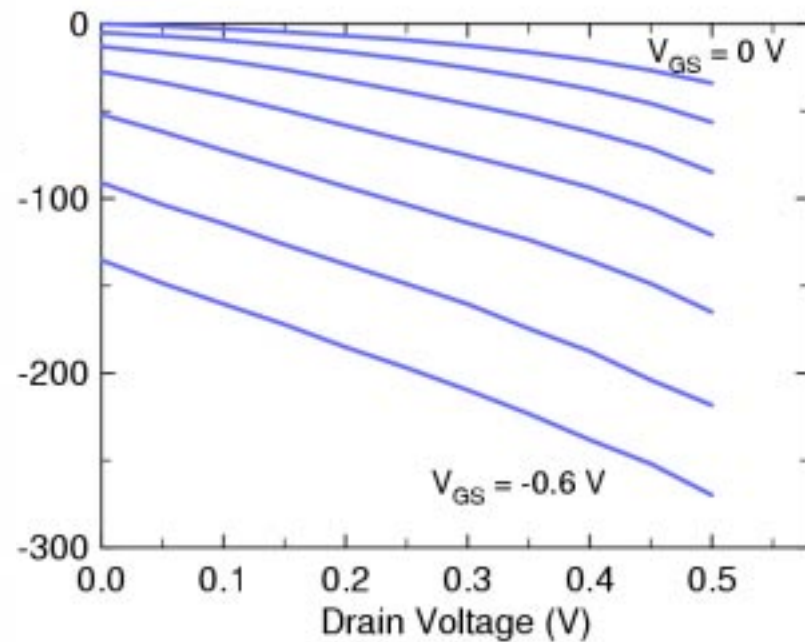


# TiW/Au Gate Leakage Current

TiW/Au gate HEMT



Cr/Au gate HEMT



- TiW/Au gate HEMTs exhibit 10x lower gate leakage current compared to previous Cr/Au gate HEMTs.
- Decrease is believed to be due to reduction in defect-assisted tunneling through the barrier.
- Gate leakage current further reduced by 10x at 77K.

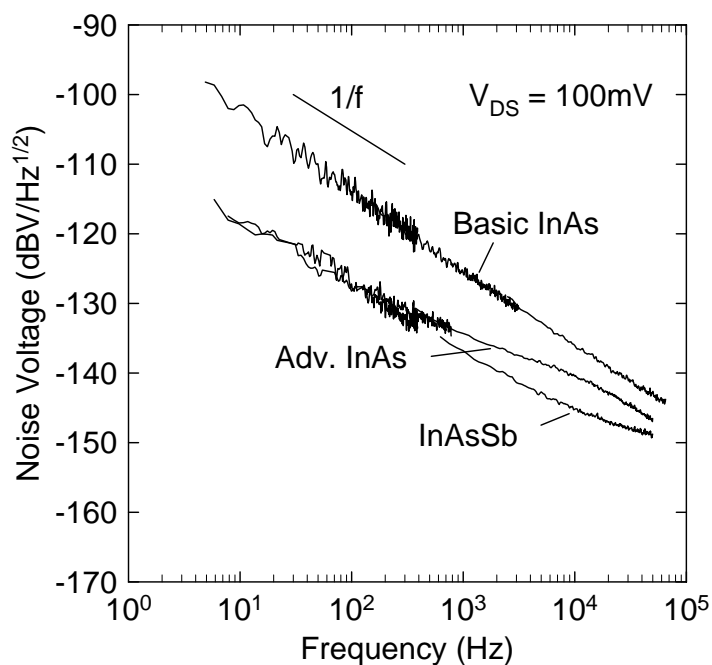
# Thermal Stability of TiW/Au HEMT

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- Heat treatment:
  - Hot plate located in  $H_2:N_2$  ambient
  - 90°C-210°C in 30°C increments
  - 1 hour duration for each heat treatment
- Only small change observed in reverse current or S-parameters until 210°C treatment.
- Cr/Au gate HEMTs on similar material showed 5-10x increase in reverse leakage current at 150°C.

# AISb/InAs HEMT

## Low-Frequency Noise Measurements



### Noise Summary

Device	$\mu$	$n_S$	$\alpha_H$
Basic	29,000	$9.0 \times 10^{11}$	$6.9 \times 10^{-3}$
Advanced	20,000	$1.9 \times 10^{12}$	$1.2 \times 10^{-3}$
InAsSb -Channel	13,400	$1.4 \times 10^{12}$	$7.5 \times 10^{-4}$

$$S_V = \alpha_H V^2 / N f$$

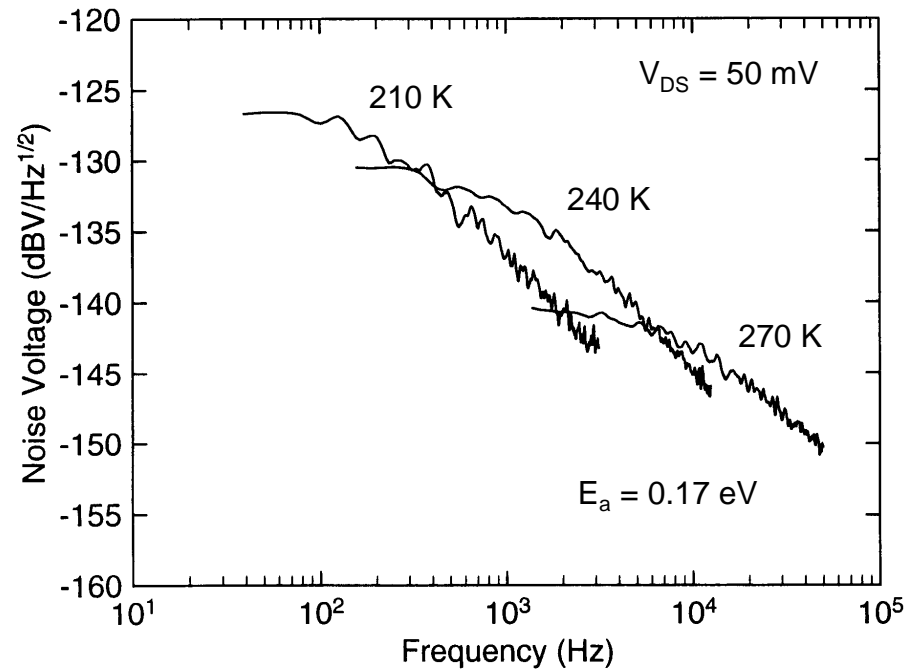
- First low-frequency noise measurements of Sb-based HEMTs.
- Hooge parameters ( $\alpha_H$ ) for three types of devices are reasonable for a relatively immature technology.

Ref: *IPRM Proceedings*, May 2000



# Low Temperature 1/f Noise Measurements

## InAsSb channel HEMT



Prominent noise bump moves down with temperature for InGaSb channel HEMT. Activation energy estimated to be 0.17 eV.

# Antimonide-Based Resonant Interband Tunneling Diode(RITD)/HEMT Logic Circuits

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- **Need**

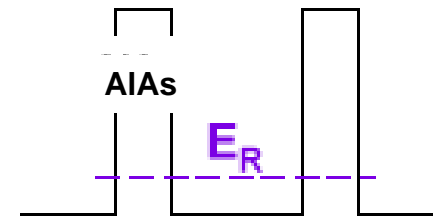
- Future multifunction radar, EW, and communication systems will require ultra-high-speed and ultra-low-power digital circuits which have reduced chip size and increased density.

- **Potential Solution**

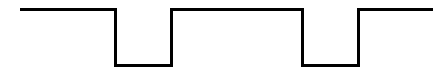
- RTDs combined with HEMTs result in high functionality, small size, low power consumption, and fast operating speed.
- Antimonide-based RITD/HEMT logic circuits have potential to set new standards for speed and power consumption.

# Advantages of Antimonide-Based RITD/HEMT Logic Circuits

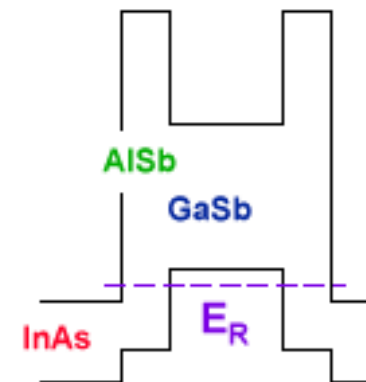
- RTDs combined with HEMTs result in high functionality, small size, low power consumption, and fast operating speed.
- Type II AlSb/InAs/GaSb RITDs are ideal for high-speed, low-power applications.
  - High peak current and low valley current at low drain voltage.
- AlSb/InAs HEMTs perform well at low drain voltage and have potential for lowest power-delay product for any semiconductor.
  - High  $f_T$ ,  $f_{max}$  at low drain voltage
  - Large current drive



InGaAs



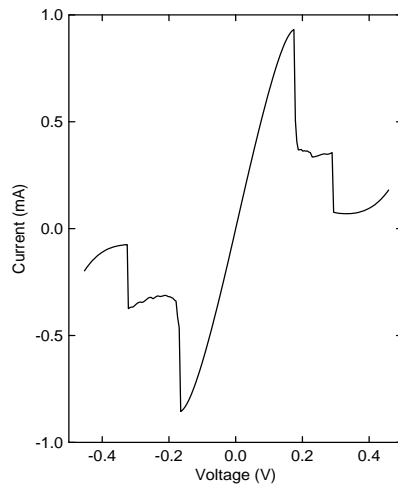
Type I RTD (InP-based)



Type II RITD (Sb-based)

# Sb-Based RITD/HEMT Logic Circuits

**RITD**

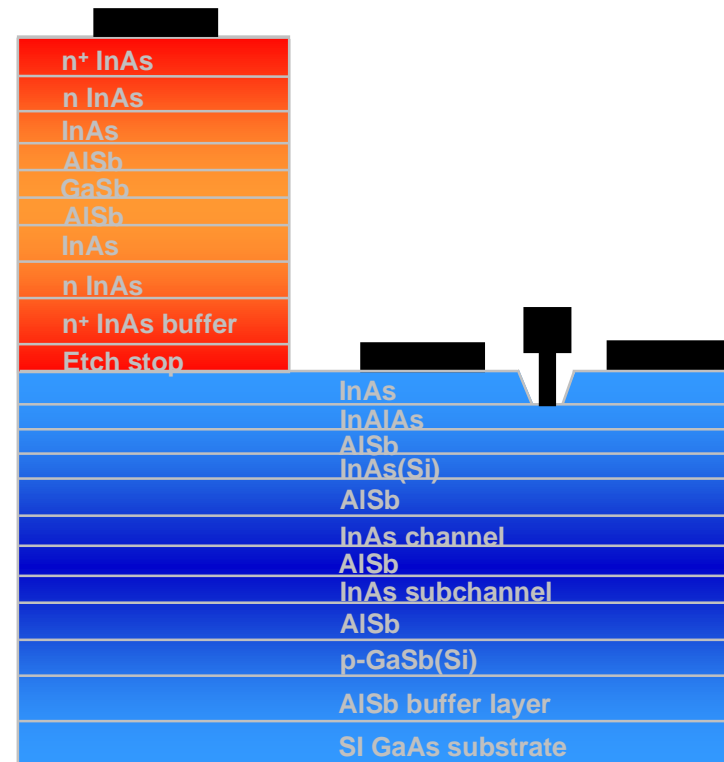
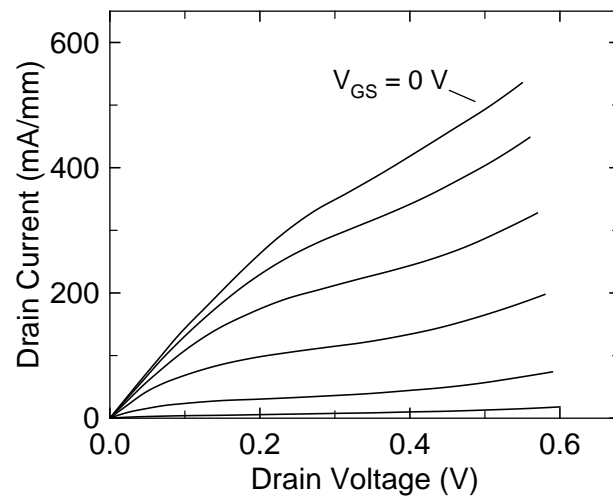


Peak current density:  $1.4 \times 10^4$  A/cm<sup>2</sup>

Peak voltage: 0.12 V

Peak-to-valley ratio: 11

**0.1  $\mu$ m HEMT**

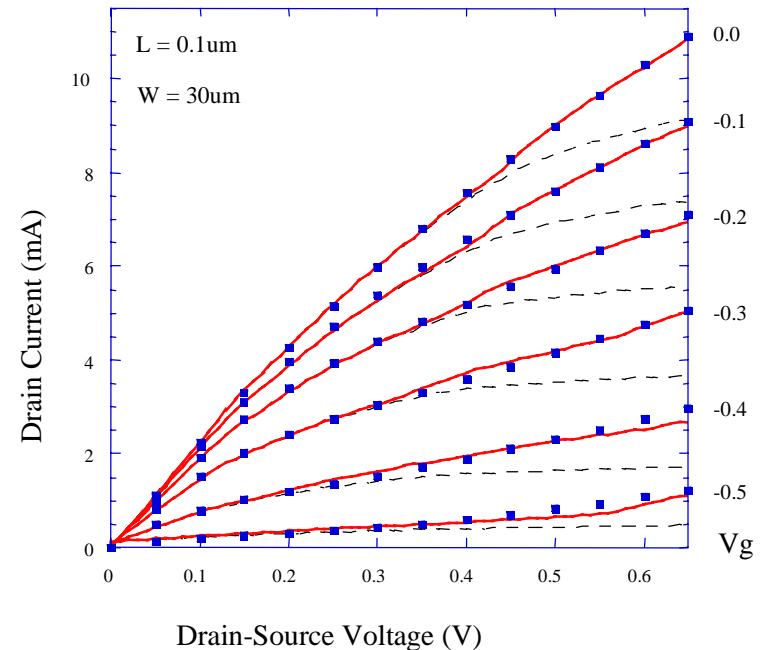
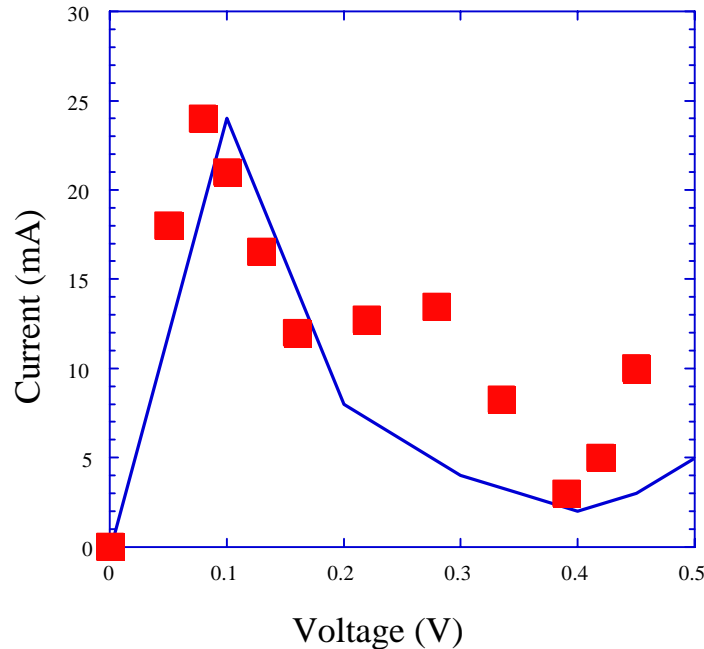


Ref: *J. Vac. Sci. Technol. B*, 18 (3), May/June 2000



# Sb-Based RITD/HEMT Simulation

**Large-signal model: dc model combined with bias-dependent small-signal equivalent circuit.**



Gm: Piecewise linear dc model

$$C_m: \frac{\epsilon A}{d + \sqrt{2\epsilon V/qN}} \text{ or } 4 \text{ fF}/\mu\text{m}^2$$

Experimental data from R. Magno (NRL)

Ref: *IPRM Proceedings*, May 2000

Phenomenological dc model:

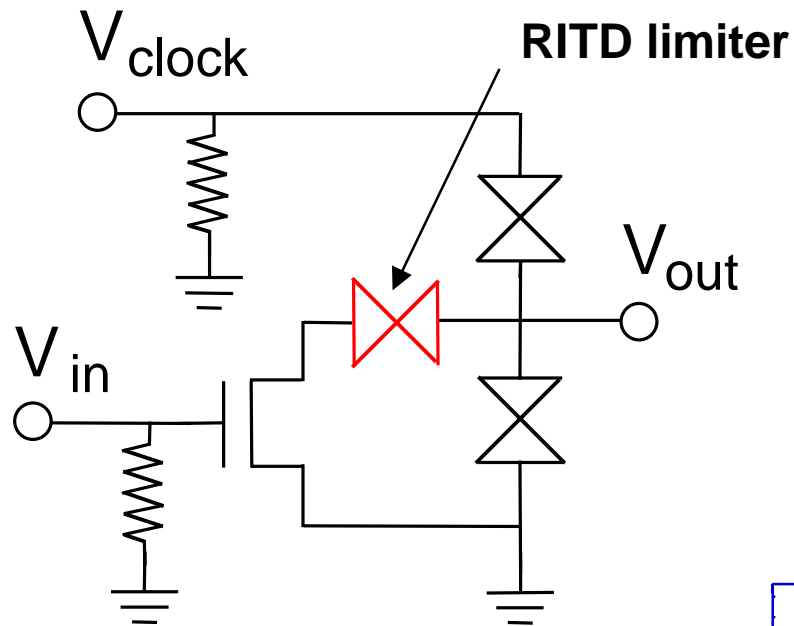
$$I_d = I_o + I_d M + \frac{TI_d M}{1 + \epsilon I_d M} \approx \frac{I_o}{1 - MT} \equiv I_o(1 + \eta)$$

$M \ll 1, \quad \epsilon I_d M \ll 1$

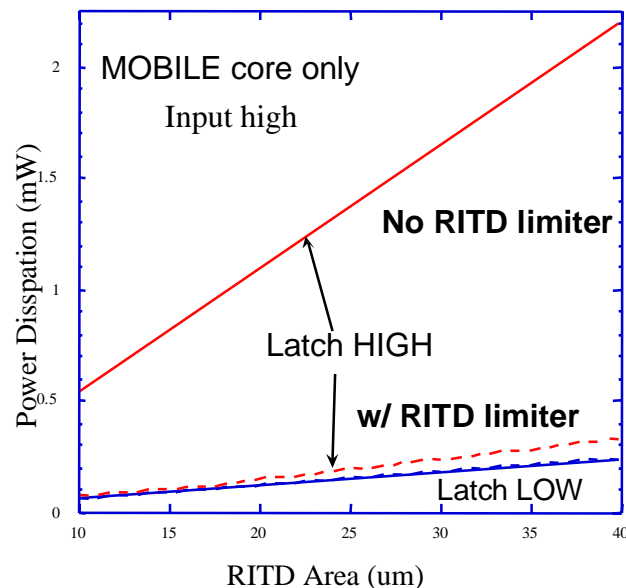
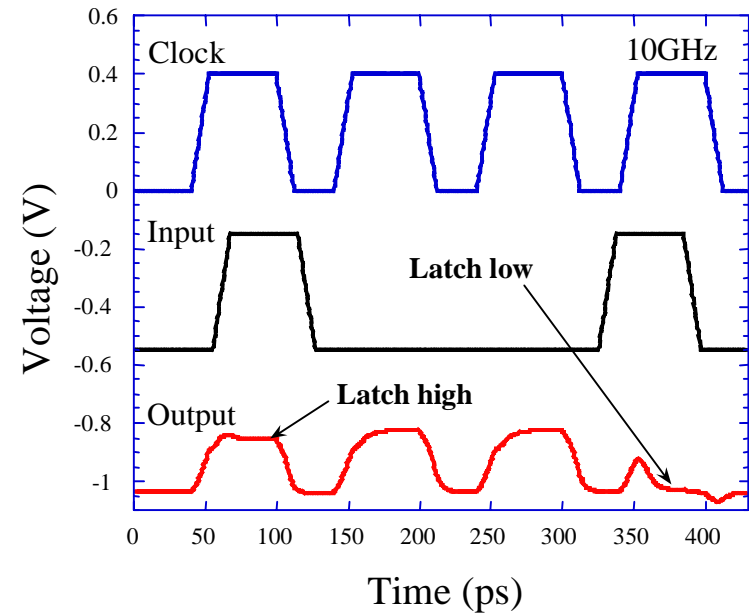
Annotations: "multiplication" points to  $I_d M$  and "trapping" points to  $\frac{TI_d M}{1 + \epsilon I_d M}$ .

# Sb-based MOBILE Circuit

## MOBILE-based flip-flop



- Addition of RITD current limiter significantly reduces power dissipation. (Pacha et al., *IEEE Trans. VLSI Syst.*, 8 (5), 2000)
- SPICE simulation of HEMT/RITD circuit predicts 5-10X lower power dissipation than comparable InP-based circuit.



SPICE  
simulations  
D-flip-flop

Static  
Power



# Gate Leakage Current Reduction using “Smart-Cut” Layer Transfer Technology

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- **Objective:**

- Fabricate and characterize Sb-based circuits on hybrid substrates to lower dislocation density.

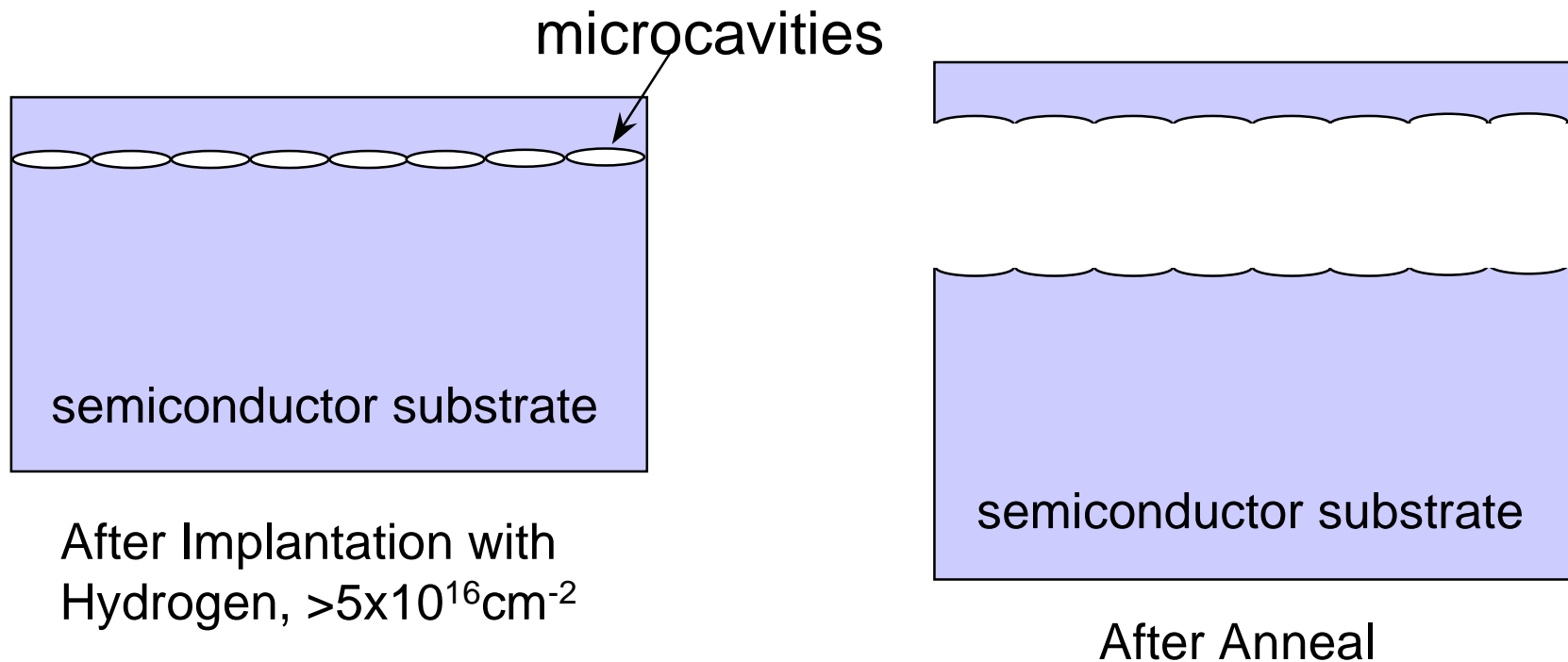
- **Plans:**

- Develop hydrogen ion-implant layer splitting process to transfer ultra-thin GaSb or InAs layers to an insulating substrate.
- Grow high-quality HEMT layers which are lattice-matched to the ultra-thin transferred material.

# “Smart-Cut” Wafer Splitting Technology

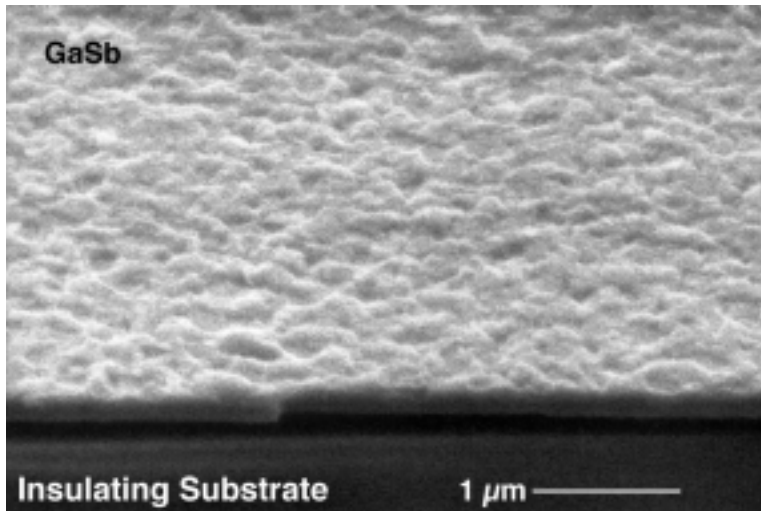
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Hydrogen gas expands when heated and splits semiconductor

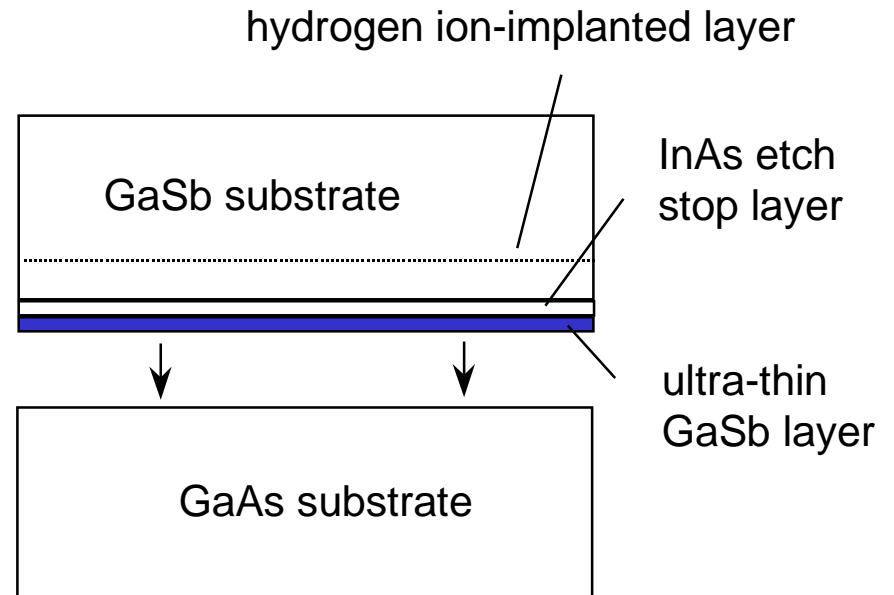


Demonstrated to date for single-crystal Si, GaAs, SiC, Ge, GaN

# “Smart-Cut” and Wafer Bonding of GaSb



SEM image of GaSb transferred to insulating substrate.



“Ultra-Cut” Process

First demonstration of wafer bonding and hydrogen ion-implant layer splitting to form ultra-thin GaSb on an insulating substrate.

Ref: *Electron. Lett.*, vol. 35, no. 8, April 1999

# Summary

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- **Demonstrated 0.1  $\mu\text{m}$  InAsSb-channel HEMTs.**
  - AlSb/InAsSb has type-I band lineup which enables more hole confinement.
  - Voltage gain of 6 is highest reported for this material system with this gate length.
- **Demonstrated 0.2  $\mu\text{m}$  InAs HEMTs with TiW/Au gate metalization.**
  - 10x reduction in gate leakage current at low drain voltage using TiW/Au gate and adjusted oxygen plasma surface pretreatment.
  - HEMTs were thermally stable to 180°C when heat treated in a  $\text{H}_2/\text{N}_2$  ambient.
- **Performed low-frequency noise measurements of Sb-based HEMTs.**
  - Hooge parameters ( $\alpha_H$ ) of  $10^{-2}$  to  $10^{-3}$  for three types of devices are reasonable for a relatively immature technology.
- **Demonstrated Sb-based RITD/HEMT integration.**
  - HEMT and RTD performance is comparable to that obtained on discrete devices.
  - Initial PSPICE simulation of HEMT/RTD MOBILE circuit predicts record 5-10X lower power dissipation than comparable InP-based circuit.
- **Demonstrated wafer bonding and hydrogen ion-implant layer splitting (“Smart Cut”) of GaSb.**
  - To be used for the growth of high-quality HEMT layers which are lattice-matched to the ultra-thin transferred GaSb material.